Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.019”**

**.019”**

**ANODE**

**.011 x .011”**

\***DO NOT BOND TO CENTER AREA\***

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .006” X .006”**

**Backside Potential: Cathode**

**Mask Ref: G23**

**APPROVED BY: DK DIE SIZE .019” X .019” DATE: 2/28/17**

**MFG: ZETEX THICKNESS: .005” P/N:BZX55C10**

**DG 10.1.2**

#### Rev B, 7/19/02